Journal of Engineering Research and Reports

9(2): 1-6, 2019; Article no.JERR.53082
ISSN: 2582-2926

Incorporating Package Grinding Process for QFN Thin Device Manufacturing

Rennier S. Rodriguez[1] and Frederick Ray I. Gomez[1*]

[1]New Product Development and Introduction, STMicroelectronics, Inc., Calamba City, Laguna, 4027, Philippines.

Authors' contributions

This work was carried out in collaboration between both authors. Both authors read, reviewed and approved the final manuscript.

Article Information

DOI: 10.9734/JERR/2019/v9i217014
Editor(s):
(1) Dr. P. Elangovan, Associate Professor, Department of EEE, Sreenivasa Institute of Technology and Management Studies, Chittoor, Andhra Pradesh, India.
Reviewers:
(1) Adegbola, Adeyinka Ayoade, Ladoke Akintola University of Technology, Nigeria.
(2) A. Ayeshamariam, Khadir Mohideen College, India.
Complete Peer review History: http://www.sdiarticle4.com/review-history/53082

Original Research Article

Received 05 October 2019
Accepted 09 December 2019
Published 02 January 2020

ABSTRACT

Package thinning, down-scaling, and miniaturization are common interests among semiconductor industries, with each manufacturing site having different approach and technical directions in providing novelties in their products. The paper offers an innovative design of manufacturing flow to reduce the semiconductor package height of a Quad-Flat No-leads (QFN) device through the application of a specialized package grinding process. The process would significantly reduce the carrier thickness for the overall package height configuration of QFN. Through this integration, the common assembly barriers and defects related in producing thin devices are eliminated, thus thinner version manufacturing becomes more simplified and efficient.

Keywords: QFN; QFN multi-row; package grinding; leadframe design.

1. INTRODUCTION

The introduction of Quad-Flat No-leads (QFN) device to surface mount technologies becomes renowned due to its advantage in cost and size compared to other packaging techniques. Most of QFN devices currently produced nowadays are demanded by mobile phones, electronic

**Corresponding author: Email: frederick-ray.gomez@st.com, f.i.gomez@ieee.org;*

wearables and laptop suppliers, which is positively moving towards cheaper yet powerful devices. To be able to adapt to this fast-changing trend [1-3], densification and thinning of integrated circuit (IC) packaging become the interest of semiconductor manufacturing companies. By producing thinner version of QFN, multiple advantages can be derived from this direction such as 1) reduced lead inductance from the internal interconnection of metal carrier and wirings, 2) good thermal and electrical performance due to thin profile between silicon die and printed circuit board (PCB) where lesser distance in between increases the thermal dissipation. Tangible benefits such as lower consumption of direct material such copper (Cu) leadframe, gold (Au) wires and molding compound may also be achieved corresponding to this direction. Common practices such as qualification of thin leadframes, reduced silicon die thickness and die attach films (DAF) material are examples of ongoing solutions among manufacturing sites in providing thinner packages together with assembly readiness of machine, indirect materials (tools such as pick-up tool and needle, grinding tool, handler, etc.) and technical competitiveness (silicon die design and architecture).

Despite its positive effect on the application and functional side, the thinner roadmap of QFN has negative interaction to structural test requirement such as delamination and reliability testing. As the package height is reduced, the amount of effective area for the mechanical interlocking of leadframes is also reduced producing weak interface between the molding material and leadframe as shown in Fig. 1. The expansion and compression of material during thermal cycle produces continuous mechanical stress on the material wherein a weak mechanical interface will result to delamination.

2. LITERATURE REVIEW AND PACKAGE DESIGN SOLUTION

A complete process flow for a standard QFN package starting from pre-assembly to back-end assembly until test and finish and packing is itemized in Fig. 2. It is worth noting that assembly and test process flow varies with the product and the technology [3-5].

The existing design of QFN, governed by assembly design rules [6-7], has an outside footprint called stand-off which is the result of etching process. The stand-off as shown in Fig. 3 occupies the 40% of the thickness of a standard multi-row QFN. The remaining 60% is the only effective area for interlocking.

Grinding process is an additional process step that will be incorporated to the standard

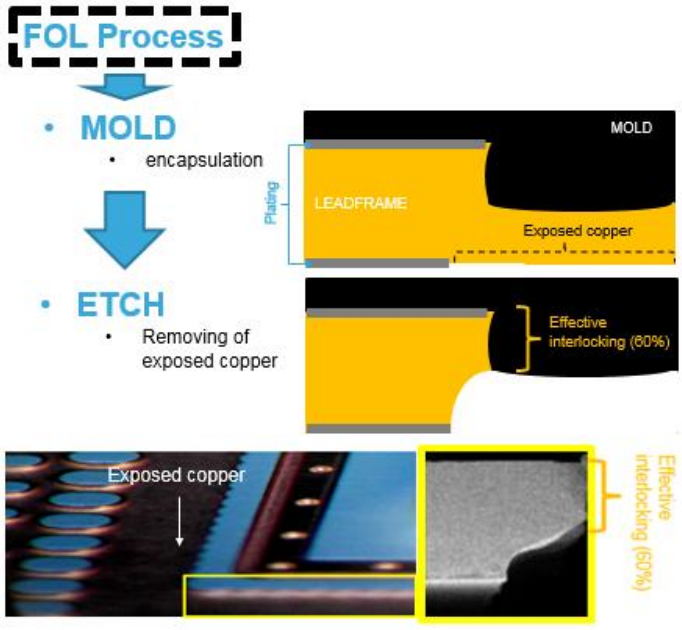

Fig. 1. Mechanical interlocking of leadframe for QFN multi-row

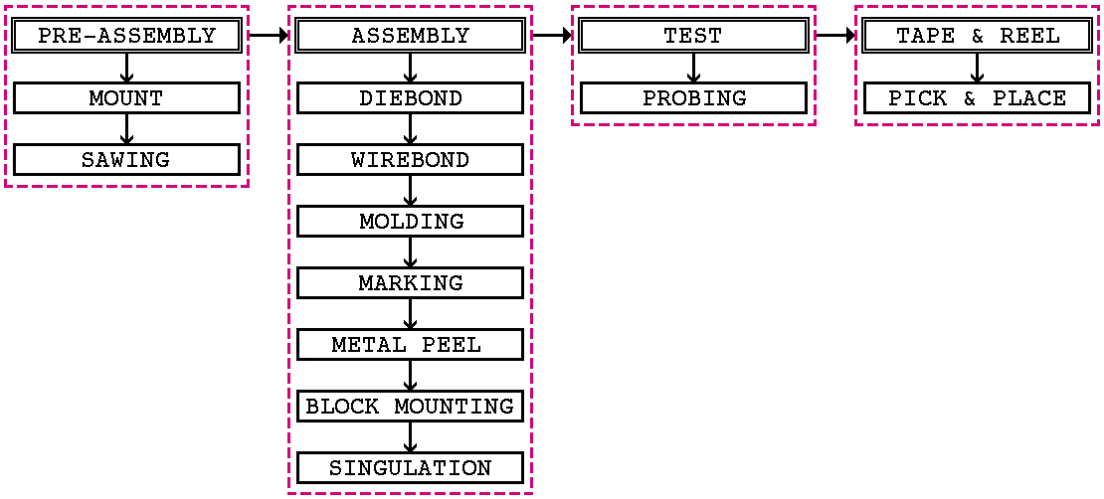

Fig. 2. Complete process flow

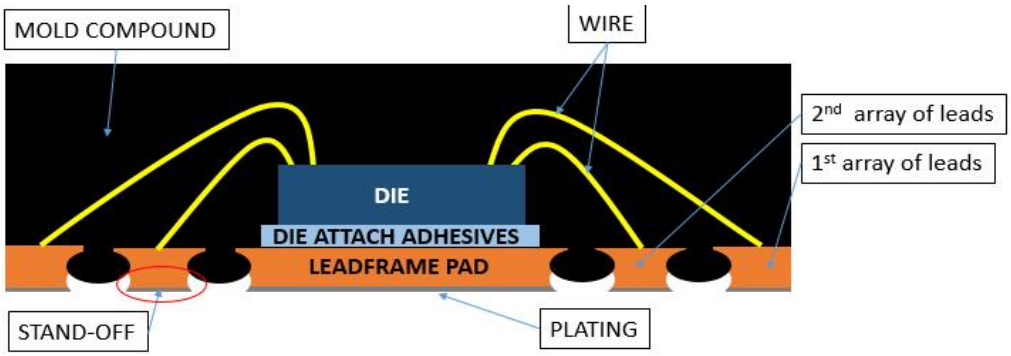

Fig. 3. Standard QFN package

manufacturing flow of integrated circuit assembly. Shown in Fig. 4 is the augmented processing of QFN with grinding process added between etching and singulation. Take note that this package grinding process is an end-of-line (EOL) process, as there is also a grinding process for wafers in front-of-line (FOL) [8-11].

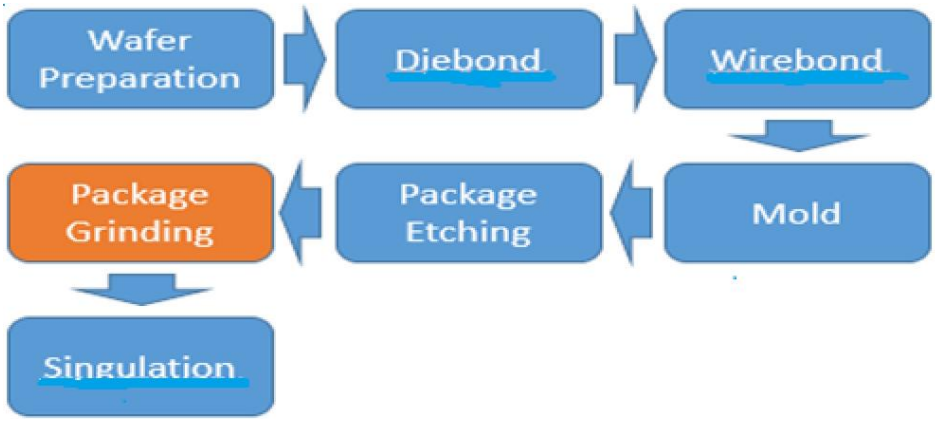

Fig. 4. Assembly process flow

Cross-sectional illustration of a QFN after the grinding process is integrated is depicted in Fig. 5. Focusing on the interlocking design, the shape of the interlocking is different as compared to the crescent design of the standard QFN.

The T-shape configuration of the novel design in Figs. 5 and 6 offers better vertical and horizontal mechanical strength which can withstand the dynamic effect of mechanical stress during thermal cycle. Fig. 6 illustrates the assembly method of the novel design. The die will be bonded on top of the carrier using semiconductor adhesives then afterwards wire will be connected from the silicon die to the arrays of leadframe leads. The overall carrier and units will be encapsulated by a molding compound and a grinding process will reduce the height of the carrier according to the defined measurement. To able to produce a wettable backside for PCB application, the backside can be plated with tin (Sn) through plating technology. On the preliminary stage of assembly (die attach, wirebond) leadframe is still thicker to lessen the potential assembly rejection related to flimsiness such as crumpled leadframe, warpage, non-stick-on-pad, and non-stick-on-lead, therefore the unit is stable during assembly.

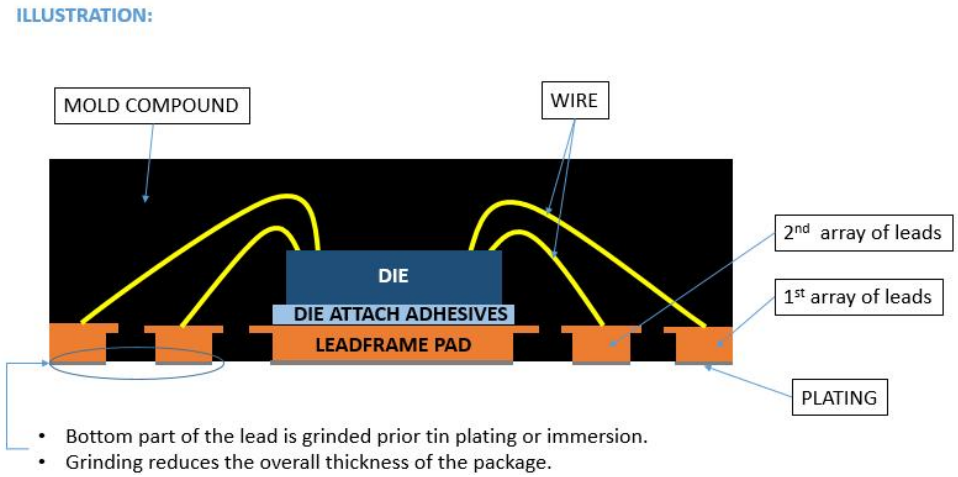

Fig. 5. QFN with grinding process

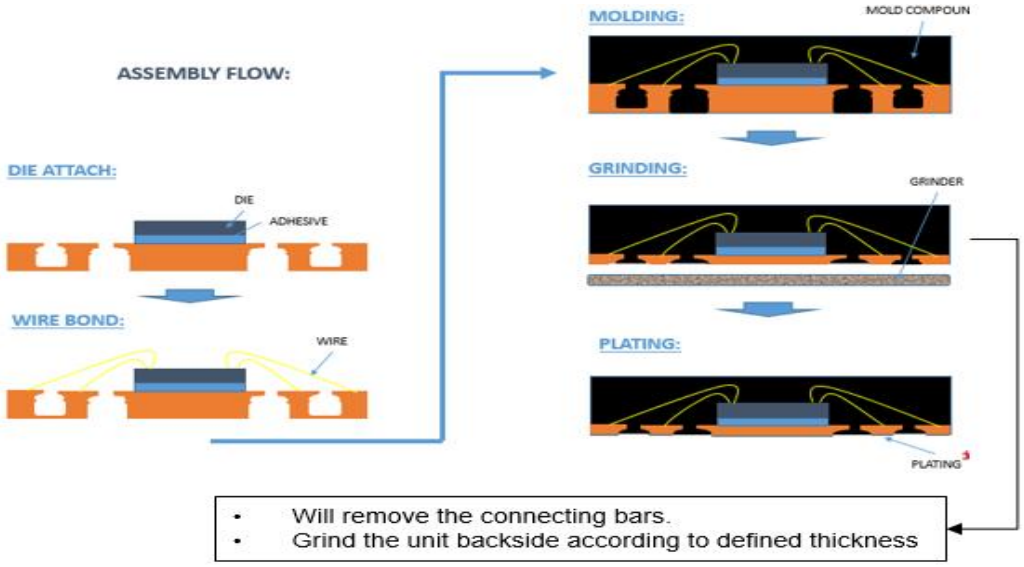

Fig. 6. Method of assembly

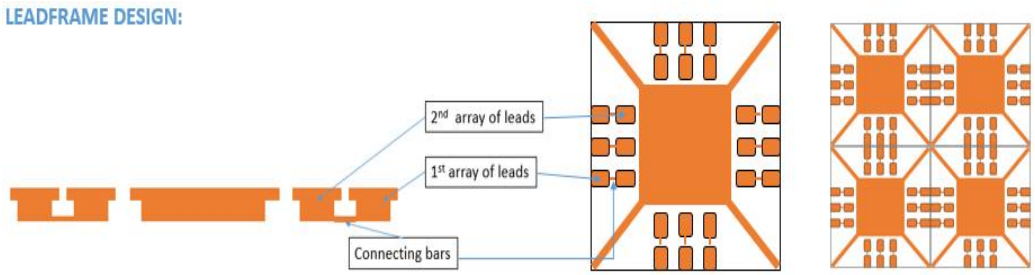

Fig. 7. Leadframe design

The specialized leadframe design is finally given in Fig. 7. The leadframe is made from copper-based material where the design of the pads and leads is done through cycle of masking, etching and plating at the side of leadframe suppliers. The connecting bars is necessary to hold the lead and pad during preliminary process of IC assembly and will be removed at the later part of the assembly.

3. CONCLUSION AND RECOMMENDATIONS

The integration of the idea presented in the paper to the existing flow of IC manufacturing was able to improve the capability for thin device processing. The limitations from the standard design is eliminated through the new design of leadframe and grinding process that is incorporated at the later part of assembly. The combination of leadframe design and grinding process also eliminates known assembly rejection related to thin device processing. Discussions in [8,11] are helpful to mitigate defects related to assembly process. Furthermore, it is worth noting that the assembly manufacturing should observe proper electrostatic discharge (ESD) checks and controls. Learnings shared in [11-13] are very helpful to realize proper and effective ESD-related controls.

DISCLAIMER

The products used for this research are commonly and predominantly used products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts of the authors.

ACKNOWLEDGEMENTS

The authors would like to express appreciation and gratitude to the New Product Development & Introduction (NPD-I) team and the Management Team of STMicroelectronics Calamba for the continuous support.

COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Tsukada Y, Kobayashi K, Nishimura H. Trend of semiconductor packaging, high density and low cost. 4th International Symposium on Electronic Materials and Packaging, Taiwan; 2002.
2. Liu Y, Irving S, Luk T, Kinzer D. Trends of power electronic packaging and modeling. 10th Electronics Packaging Technology Conference, Singapore; 2008.
3. Doering R, Nishi Y. Handbook of semiconductor manufacturing technology. 2nd ed., CRC Press, USA; 2007.
4. Geng H. Semiconductor manufacturing handbook. 1st ed., McGraw-Hill Education, USA; 2005.
5. May GS, Spanos CJ. Fundamentals of semiconductor manufacturing and process control. 1st ed., Wiley-IEEE Press, USA; 2006.
6. STMicroelectronics. Assembly and EWS design rules for wire bond Interconnect dice. rev. 53.0; 2018.
7. STMicroelectronics. Advanced EWS and assembly design rules specification. rev. 34.0; 2018.
8. Bacquian BC, Gomez FR. A study of wafer backgrinding tape selection for SOI wafers. Journal of Engineering Research and Reports. 2019;6(2):1-6.

9. Combs E. The back-end process: Step 3 - Wafer backgrinding; 2002.
10. "Wafer breakage due to backgrinding", The Cutting Edge Technical Newsletter; 2008.
11. Sumagpang A, Gomez FR. A methodical approach in critical processes optimization of new scalable package semiconductor device for ESD applications. Asian Journal of Engineering and Technology. 2018; 6(6):78-87.
12. Gomez FR. Improvement on leakage current performance of semiconductor IC packages by eliminating ESD events. Asian Journal of Engineering and Technology. 2018;6(5).
13. Gomez FR, Mangaoang T. Elimination of ESD events and optimizing waterjet deflash process for reduction of leakage current failures on QFN-mr leadframe devices. Journal of Electrical Engineering, David Publishing Co. 2018;6(4):238-243.

Peer-review history:
The peer review history for this paper can be accessed here:
http://www.sdiarticle4.com/review-history/53082