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An Efficient CRT Based Reverse Converter for $\{2^{2n+1}-1, 2^{n-1}, 2^{2n}-1\}$ Moduli Set

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Authors' contributions

This work was carried out in collaboration between authors HKB and KAG. Both authors read and approved the final manuscript.

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Abstract

This paper presents a reverse converter for the moduli set $\{2^{2n+1}-1, 2^{n-1}, 2^{2n}-1\}$ using a Chinese Remainder Theorem (CRT) algorithm and reverse method of data conversion. We compare our result with other converters found in literature that have the same Dynamic Range (DR) and our proposed algorithm has a better performance in terms of speed.
Aims: The aim of this study is to design a reverse converter for the moduli set $\{2^{2n+1}-1, 2^{n-1}, 2^{2n}-1\}$, determine the speed and compare it with other moduli set with the same DR in literature.
Methodology: We applied Chinese Reminder Theorem algorithm for data conversion.

Keywords: Reverse converter; moduli set; Chinese remainder theorem; dynamic range; data conversion.

1 Introduction

Residue Number System (RNS) is an unconventional number system with high potential for accelerating the speed of arithmetic operations. The implementation of addition and multiplication in parallel and fast architecture is possible in RNS due to its inherent carry-free properties [1,2]. In addition to these properties, it has also received a considerable attention in literature due to its modularity and fault tolerance [3]. The

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RNS is considered as one of the efficient alternative number system capable to increase the speed in hardware implementation of Digital Signal Processing (DSP) [4-6].

Many moduli sets are in use in RNS with different Dynamic Range (DR). The most popular 3n-bit DR moduli set known as traditional moduli set is $\{2^n-1, 2^n, 2^n+1\}$ [7]. Others are $\{2^{n-1}, 2^n-1, 2^n+1\}$, $\{2^{n-1}-1, 2^n-1, 2^n\}$ [8]. The dynamic range of 3n-bits produced by this moduli set will not be able to be used by any application with higher DR. 4n-bit DR 4 moduli set such as $\{2^n-1, 2^n, 2^n+1, 2^{n+1}+1\}$, $\{2^n-1, 2^n, 2^n+1, 2^{n+1}-1\}$, $\{2^n-1, 2^n, 2^n+1, 2^{n-1}-1\}$ [9] were suggested. In order to raise parallelism in RNS arithmetic, 5n-bit moduli set were suggested $\{2^n, 2^{2n}-1, 2^{2n}+ 1\}$, $\{2^n-1, 2^n, 2^n+1, 2^{2n}+1\}$ etc. were also proposed [10].

RNS is gaining popularity among RNS researchers, but not widely used because of the following problems (i) sign detection, (ii) magnitude comparison, (iii) overflow detection (iv) Conversion from residue number to binary number etc.

The objective of this paper is to address the conversion issue by designing a RNS converter with high speed and compare it with similar converters on the state of the art with the same dynamic range.

RNS has three main parts; binary to residue conversion (forward conversion), arithmetic operations and residue to binary conversion (reverse conversion) [7]. Obviously, RNS to Binary conversion is either based on Chinese Remainder Theorem (CRT) or Mixed Radix Conversion (MRC) [11-15]. In this paper we discuss a reverse conversion using Chinese Remainder Theorem method. The rest of this paper is organized as follows: In section 2, we give a background to RNS, in section 3, we discuss the proposed converter, in section 4 we present the hardware realization, in section 5 we discuss the performance evaluation and finally we give the conclusion of the paper in section 6.

2 Background

Residue Number System (RNS) is the representations of a large integer number with a set of smaller integer numbers in order to make computation fast and efficient. RNS history may be traced back to 1599 years; it begins with a Chinese Scholar, Sun Tzu [16] with Chinese riddle as follows: What is the number such that when divided by 7, 5 and 3 will have the remainders of 2, 3 and 2 respectively? The procedure of obtaining the solution to the riddle is known as Chinese Remainder Theorem (CRT).

2.1 RNS representation

Residue Number System is defined by a set of relatively prime integers called the moduli. The moduli set is represented as $\{m_1, m_2, m_{3\dots} m_n\}$ where m_k is the k^{th} modulus. Each integer can be represented as a set of smaller integers called the residue [17]. The residue numbers are represented by $\{r_1, r_2, r_3, \dots r_n\}$ where r_k is the k^{th} residue. The residue r_k is defined as the least positive remainder when X is divided by the modulus m_i. The RNS of X with respect to the moduli m_i is denoted by $|X|_{mi} = r_i$

Dynamic range in RNS is the product of all the moduli sets denoted by $M = \pi^n_{i=1} m_i$ i.e. $M = m_1 m_2 m_{3\dots} m_n$ [18]. An RNS with a dynamic range M will have a unique representation between 0 and M-1 [19]

2.2 Data conversion methods

Data conversion is an important topic in RNS. Data need to be converted from binary to RNS before any operation can be performed on them. However, the success of hardware realization depends on both data conversion and choice of moduli. Data conversion is divided into two categories: (i) Forward conversion and (ii) Reverse conversion.

Forward conversion: This is the conversion of binary number to RNS. In binary system, forward conversion can be represented as

$$|x_m| = |\sum^{n-1}_{j=0} b_j 2^j|_m$$

For any n-bit non negative integer X in the range $0 < x \geq 2^n-1$, the hardware computation of forward conversion is based on Look up Table (LUT) [20].

2.3 Reverse conversion in residue number system

Reverse conversion is the conversion of residue number system to a conventional number (binary numbers). Reverse conversion is one of the complex parts of RNS [21]. The success of reverse conversion depends on forward conversion [22]. Reverse conversion is based on two popular algorithms: Chinese Remainder Theorem (CRT) [23,24] and Mixed Radix Conversion (MRC) [25] algorithms. The use of CRT entails a large modular adder whereas MRC is a sequential process that requires a number of Look–Up Table (LUT) [26].

The Chinese Remainder Theorem is a very useful algorithm for reverse conversion; it assumes that a number will have a unique representation in RNS if we chose appropriate moduli for the RNS. The algorithm involves computation of inverse and is given by

$$X= |\Sigma^n_{i=1}|x_i M_i^{-1}|_{mi} M_i |_M$$

2.4 Moduli choice

The following points are to be carefully considered in the choice of RNS moduli

- The moduli must be relatively primed.
- The smaller the moduli, the faster the arithmetic operations.
- To avoid overflow, the dynamic range should be large enough.
- Efficiency of the RNS moduli should be considered and high efficiency is more desirable, example the RNS (15|13|11) require 12 bits it can represent $2^{12} = 4096$, whereas only 2145. numbers are presented the efficiency is 52%.
- Select prime numbers in sequence until a desired dynamic range is obtained.
- Moduli numbers can be restricted to power of 2.

3 The Proposed Algorithm

In this section, we proposed a reverse converter algorithm for the moduli set $2^{2n+1}-1.\ 2^{n-1}, 2^{2n}-1$ using Chinese Remainder Theorem (CRT).

If we assume $m_1 = 2^{2n+1}-1$, $m_2= 2^{n-1}$ and $m_3 = 2^{2n}-1$ then, the following theorem hold to be true:

Theorem 1: The moduli set $\{2^{2n+1} – 1, 2^{n-1}, 2^{2n}-1\}$ are pairwise relatively prime numbers

Proof: Using Euclid's theorem $\gcd (m_1,m_2) = \gcd(m_2, |m_1|_{m2}) = 1$

$\gcd (2^{2n+1} – 1, 2^{n-1}) = \gcd(2^{n-1},| 2^{2n+1} – 1|_2{}^{n-1})$

$= \gcd(2^{n-1}, -1) = 1$

Then, $\gcd (2^{2n+1} – 1, 2^{2n}-1) = \gcd(2^{2n}-1,|2^{2n+1} – 1|_{2^{2n}-1})$

To evaluate $|2^{2n+1} – 1|_{2^{2n}-1}$

$$\begin{aligned}|2^{2n+1} – 1|_{2^{2n}-1} &= |2^{2n+1} |_{2^{2n}-1} \ |– 1|_{2^{2n}-1} \\ &= |2 \text{ x } 2^{2n}|_{2^{2n}-1} - |– 1|_{2^{2n}-1} \\ &= |2|_{2^{2n}-1} \text{ x } 2^{2n}|_{2^{2n}-1} - 1 \\ &= 2 \text{ x } |_2{}^{2n}-1 + 1 |_{2^{2n}-1} -1 \\ &= 2 – 1 \\ &=1\end{aligned}$$

Implies $\gcd(2^{2n}-1, 1) = 1$

Also
$gcd(2^{2n} - 1, 2^{n-1}) = gcd(2^{n-1}, |2^{2n} - 1|_{2^{n-1}})$
if $|2^{2n} - 1|_{2^{n-1}} = -1$
then $gcd(2^{n-1}, |2^{2n} - 1|_{2^{n-1}}) = gcd(2^{n-1}, -1) = 1$

By the above proof, it is confirmed that $2^{2n+1} - 1$, 2^{n-1}, $2^{2n}-1$ are relatively prime since the greatest common divisor (gcd) are 1. Therefore, our proposed moduli set can be used in RNS and we can proceed to determine its reverse converter.

The confirmation of Theorem 1, is an assurance that our proposed moduli set can be used in RNS. We can therefore proceed to design its reverse converter.

Lemma 1: The residue of a negative number in modulo $(2^k -1)$ is the one's complement of t where $0 \leq t < 2^k -1$.

Lemma 2: The multiplication of a residue number t by 2^s in modulo $(2^k -1)$is carried out by k bit circular left shift where s is a natural number [27]

Let our $m_1 = 2^{2n+1} - 1$, $m_2 = 2^{n-1}$, $m_3 = 2^{2n}-1$, The CRT is given by

$$X = \left|\sum_{i=1}^{n} |x_i M_i^{-1}|_{mi} M_i \right|_M \tag{1}$$

$$\text{where } M_i = \pi_{i=1}^{n} m_i;\ M_i = \frac{M}{mi};\ |M_1^{-1} \times M_1| = 1 \tag{2}$$

$$M_1 = \frac{M}{m1};\ M_2 = \frac{M}{m2};\quad M_3 = \frac{M}{m3} \tag{3}$$

Theorem 2: Given the moduli set $2^{2n+1} - 1$, 2^{n-1}, $2^{2n}-1$ where $m_1 = 2^{2n+1} - 1$, $m_2 = 2^{n-1}$, $m_3 = 2^{2n}-1$, the following hold to be true:

$$|M_1^{-1}|m_1 = -2^{n+3} \tag{4}$$

$$|M_2^{-1}|m_2 = 1 \tag{5}$$

$$|M_3^{-1}|m_3 = 2^{n+1} \tag{6}$$

Proof

(i) Equation (4) is true only if we can demonstrate that $(2^{n-1})(2^{2n}-1)(-2^{n+3}) = 1$ w.r.t $2^{2n+1} - 1$

$$|(2^{n-1})(2^{2n}-1)(-2^{n+3})|_{2^{2n+1}-1} = (2^{2n}-1)(-2^{2n+2})|_{2^{2n+1}-1}$$
$$= |(2^{-1}2^{2n+1}-1)|_{2^{2n+1}-1} (-2^1 2^{2n+1})|_{2^{2n+1}-1}$$
$$= |((2^{-1}2^{2n+1}-1+1)-1)|_{2^{2n+1}-1} (-2^1 2^{2n+1}-1+1)|_{2^{2n+1}-1}$$
$$= (2^{-1}(1)-1)(-2^1)$$
$$= (-2^{-1})(-2^1)$$
$$= 1.$$

(ii) Equation (5) is also true only if we can demonstrate that $(2^{2n+1}-1)(2^{2n}-1)(1) = 1$ w.r.t 2^{n-1}

$$|(2^{2n+1}-1)(2^{2n}-1)|_{2^{n-1}} = (2^1 2^n 2^n-1)(2^n 2^n-1)|_{2^{n-1}}$$
$$= |(2^1 2^1 2^1 2^{n-1} 2^{n-1})-1)(2^1 2^1 2^{n-1} 2^{n-1}-1)|_{2^{n-1}}$$
$$= (0-1)(0-1)$$
$$= (-1)(-1)$$
$$= 1$$

(iii) Equation (6) is also true only if we can demonstrate that $(2^{2n+1}-1)(2^{n-1})(2^{n+1}) = 1$ w.r.t $2^{2n}-1$

$$|(2^{2n+1}-1)(2^{n-1})(2^{n+1})|_{2^{2n}-1} = |(2^{2n+1}-1)(2^{2n})|_{2^{2n}-1}$$
$$= |((2^1(2^{2n}-1+1)-1)|_{2^{2n}-1})(2^{2n}-1+1)|_{2^{2n}-1}$$

$$=|(2^1(1)-1)(1)$$
$$=2-1$$
$$=1$$

From equation (1)

$X = |\sum^n_{i=1}|x_i M_i^{-1}|_{mi} M_i|_M = \sum^n_{i=1} M_i^{-1}|_{mi}$ x X_i - M x K

$M = (2^{2n+1} - 1)(2^{n-1})(2^{2n}-1)$

$M_1 = (2^{n-1})(2^{2n}-1)$

$M_2 = (2^{2n+1} - 1)(2^{2n}-1)$

$M_3 = (2^{2n+1} - 1)(2^{n-1})$

$X = |(m_2 m_3 M_1^{-1} X_1) + (m_1 m_3 M_2^{-1} X_2) + (m_1 m_2 M_3^{-1} X_3)|_M$ - M x K

$$=[(2^{n-1})(2^{2n}-1)(-2^{n+2})X_1 + (2^{2n+1}-1)(2^{2n}-1)(1)X_2 + (2^{2n+1}-1)(2^{n-1})(2^{n+1})X_3] - M \times K$$
$$=|(-2^{4n+2}+2^{2n+2})X_1 + (2^{4n+1} - 2^{2n+1} - 2^{2n}+1)X_2 + (2^{4n+1} - 2^{2n})X_3|_M - M \times K$$
$$=|(-2^{4n+2}+2^{2n+2})X_1 + (2^{4n+1} - 2^{2n+1} - 2^{2n}+1)X_2 + (2^{4n+1} - 2^{2n})X_3|_M - (2^{n-1})(2^{2n+1} - 1)(2^{2n}-1) \times K$$
$$=2^{n-1}\{(-2^{3n+3}+ 2^{n+3})X_1 + (2^{3n+2} -2^{n+2} - 2^{n+1} + 2^{1-n}) X_2 + 2^{3n+2} -2^{n+1}) X_3\} - (2^{2n+1} - 1)(2^{2n}-1) \times K$$

By computing the floor values in modulo 2^{n-1}

$$\left\lfloor \frac{X}{2^{n-1}} \right\rfloor = [(-2^{3n+3}+ 2^{n+3})X_1 + (2^{3n+2} -2^{n+2} - 2^{n+1} + 2^{1-n}) X_2 + 2^{3n+2} -2^{n+1}) X_3]_{M'} \quad (7)$$

where $M' = (2^{2n+1} - 1)(2^{2n}-1)$

$$\left\lfloor \frac{X}{2^{n-1}} \right\rfloor = |(-2^{n+3})(2^{2n}-1) X_1 + (2^{2n}-1)(2^{n+2} - 2^{1-n})X_2)|_{M'} + (2^{3n+2}-2^{n+1}) X_3|_{M'}$$
$$= |(-2^{n+3})X_1|_{M'} + |2^{n+2} - 2^{1-n)}X_2|_{M'} + |(2^{3n+2}-2^{n+1)}X_3|_{M'} \quad (8)$$

For hardware convenience, let compute the value of $\left\lfloor \frac{X}{2^{n-1}} \right\rfloor$ using

$$X = \left\lfloor \frac{X}{2^{n-1}} \right\rfloor \times 2^{n-1} - X_i \quad (9)$$

Form (11) let,

$$P1 = |-2^{n+3}X_1|_{M'} \quad (10)$$

$$P2 = |(2^{n+2} - 2^{n-1}) X_2|_{M'} \quad (11)$$

$$P3 = |(2^{3n+2} - 2^{n+1}) X_3|_{M'} \quad (12)$$

$$\left\lfloor \frac{X}{2^{n-1}} \right\rfloor = P1 + P2 + P3 \quad (13)$$

For effective implementation of our hardware, we simplify equations (10), (11) and (12) further.

3.1 Evaluation of P1, P2 and P3

By applying lemma 2 in the modulo lemma 2 in modulo $M' = (2^{2n+1}-1)(2^{2n}-1)$

The bit representations of our residues x_1,x_2 and x_3 are as follow:

$$P1 = |-2^{n+3}X_1|_{M'} = \underbrace{\underbrace{11..11}_{n+3}\ \underbrace{x_{1,2n},x_{1,2n-1},\ldots x_{1,1}x_{1,0}}_{2n+1}}_{4n+1}\ \underbrace{111..1111}_{n-3} \quad (14)$$

$P2 = |(2^{n+2} - 2^{n-1})X_2|_{M'}$

P2 is divided into two parts as

$P21 = |(2^{n+2} X_2|_{M'}$

$$= \underbrace{\underbrace{00\ldots00}_{n+2}\,\underbrace{x_{1,n-2}x_{1,n-3}\ldots x_{1,1}x_{1,0}}_{n-1}\,\underbrace{000\ldots00}_{2n}}_{4n+1} \quad (15)$$

$P22 = |-2^{n-1}X_2|_{M'}$

$$= -\underbrace{\underbrace{000\ldots00}_{n-2}\,\underbrace{x_{1,n-2}x_{1,n-3}\ldots x_{1,1}x_{1,0}}_{n-2}\,\underbrace{000\ldots00}_{2n+3}}_{4n+1}$$

$$\underbrace{\underbrace{111\ldots111}_{n-2}\,\underbrace{x_{1,n-2}x_{1,n-3}\ldots x_{1,1}x_{1,0}}_{n-2}\,\underbrace{111\ldots111}_{2n+3}}_{4n+1}$$

$P3 = |(2^{3n+2} - 2^{n+1})X_2|_{M'}$

P3 is also divided into two namely P31 and P32 represented below

$P31 = |(2^{3n+2} X_2|_{M'} = 000\ldots00\, x_{3,2n-1}x_{3,2n-2}\ldots x_{3,1}x_{3,0}\, 000\ldots00$

$$= (\underbrace{000\ldots00}_{n+1} + \underbrace{00\ldots00}_{2n+1})\,\underbrace{x_{3,2n-1}x_{3,2n-2}\ldots x_{3,1}x_{3,0}}_{2n}$$

$$= \underbrace{\underbrace{00\ldots00}_{2n+1})\,\underbrace{x_{3,2n-1}x_{3,2n-2}\ldots x_{3,1}x_{3,0}}_{2n}}_{4n+1}$$

$P32 = |-2^{n+1} X_3|_{M'}| = -\, 000\ldots00\, x_{3,2n-1}x_{3,2n-2}\ldots x_{3,1}x_{3,0}\, 000\ldots00$

$$= \underbrace{\underbrace{111..11}_{n+1}\,\underbrace{x_{3,2n-1}x_{3,2n-2}\ldots x_{3,1}x_{3,0}}_{2n}\,\underbrace{111..11}_{n}}_{4n+1}$$

4 Hardware Realization

The hardware implementation of the proposed Reverse converter is based on equations (10), (11), (12) and (13). The variables P1, P2 and P3 are added by carry save adder (CSA) to produce C and S. The carry propagation is used to add C and S which finally produced the final result as seen in Fig. 1.

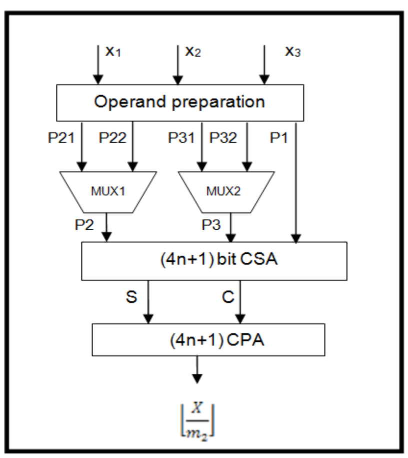

Fig. 1. Architecture of the proposed converter

5 Performance Evaluation and Comparison

The primary digital characteristics of any digital design are the speed, area and power. Latency is the time between the data input and the processing data output while, timing is the logical delay between elements. When a design doesn't meet timing, it means that the delay of the critical path is larger than the target clock period [28]. Since our architecture is CRT based, therefore, it eliminates intermediate binary stage in the proposed architecture and our architecture facilitates the implementation of RNS based processor by reducing the latency and the complexity introduced by binary stage..

In order to evaluate the performance of the proposed reverse converter, we compare it with similar best known reverse converters. The dynamic range of the proposed converter is 5n bits and is compared with other converters in literature with the same dynamic range. The comparison considered four converters; it compares our converter with each as can be seen in Table 1. The proposed converter has a better performance in term of speed than [19,13]. Also [12] has the same delay with our converter and lastly [3] is better than our proposed converter.

Table 1. Table of comparison

Converter	Number of Moduli set	Dynamic Range	Delay	Remark
The proposed Converter	3	5-n bit	8n+3	The proposed Converter
[19]	3	5n-bit	10n+13	The proposed converter is better
[13]	3	5-n bit	8n+4	The proposed converter is better
[12]	4	5-n bit	8n+3	Same with the proposed converter
[3]	3	5-n bit	8n+1	Better than the proposed converter

6 Conclusion

In this paper, a reverse converter for three moduli set $\{2^{2n+1}-1, 2^{n-1}, 2^{2n}-1\}$ with 5n-bit dynamic range based on CRT is presented. Comparison of our proposed reverse converter with some converters in literature that have the same dynamic range [19,13] showed that our proposed reverse converter gives a better performance in term of speed. However, it will be of future research interest to describe the scheme on VHDL and carry out the implementation on Field Programmable Gate Array (FPGA).

Competing Interests

Authors have declared that no competing interests exist.

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